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Implementation of Adders Using Ultra Low Power Optimization Techniques

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***Abstract*—Adders are the momentous basic building blocks used intermittently in microprocessor, digital signal processors, data processing ASICs. We can perform all types of other arithmetic operations only by using adders. In this paper we implemented adders using conventional CMOS and by using GDI technique. GDI technique is used for implementation of a wide range of complex logic functions with high speed, reduced complexity low power and area as prevalence characteristics. We also applied ultra-low power optimization techniques like multiple threshold (MTCMOS) and Low Power State Retention Technique [LPSR] to minimize the power. All this adders are implemented in DSCH simulation tool and compared power for all the implementations in MICROWIND.**

***Index terms* — carry save adder, carry skip adder, full adder, MTCMOS, LPSR technique**

I. INTRODUCTION

Most of the VLSI applications, such as DSP, image and video processing and microprocessors extensively use adders addition but also other basic arithmetic operations like subtraction, multiplication, division, increment/decrement etc. Thus, design of an efficient adder is required for better performance of the system. The consequential growth in portable systems like laptops has strengthened the research
efforts in low power VLSI circuits. The advances in VLSI technology allow hardware realization of most computing profound applications such as multimedia processing, DSP, to enhance the speed of operation [1]. Moreover, with increasing demand and the popularity of portable electronic products, the researchers are driven to strive for smaller silicon area, higher
speed, longer battery life and enhanced reliability.

The importance of digital computing lies on efficient design of adders. The main design criteria for adders are size, area, speed and power. However, they have a contradictory relationship with each other. Therefore, power delay product or energy consumption per operation has been introduced to accomplish optimal design trade-offs. The performance of digital circuits can be optimized by proper selection of logic styles.[2] Different logic styles tend to favor the accomplishment of one performance aspect at the expense of others. The main contribution of this paper presents the design of adders like ripple carry adder, carry skip adder, carry save adder and carry look ahead adder at circuit level implemented based on the GDI technique and CMOS.GDI technique offers low power, less transistor
count and high speed compared to conventional CMOS but the problem lies on fabrication process. Along with this we also used advanced power optimization techniques like MTCMOS (multiple threshold
CMOS) and Low Power State Retention (LPSR) techniques for reducing the power.

The organization of the paper is as follows: The section II, describes the design of GDI Cell and ultra power optimization techniques MTCMOS and LPSR technique. Section III, presents the implementation of different adders using GDI technique along with advanced power optimization techniques. Section IV presents the comparison of different parameters by using simulation results. Finally the conclusion is presented in section VI.

II. POWER OPTIMIZATION TECHNIQUES

A.GDI technique

It is a power efficient technique for digital circuits. The basic cell remembers the standard CMOS inverter[3]. The three primary differences are (1) It contains three inputs G common gate input of NMOS and PMOS P input to the source or drain of PMOS (2) N input to the source or drain of NMOS, (3) bulks of both NMOS and PMOS are connected to Nor P respectively, so that it can be readily biased in contrast with a CMOS inverter[4].

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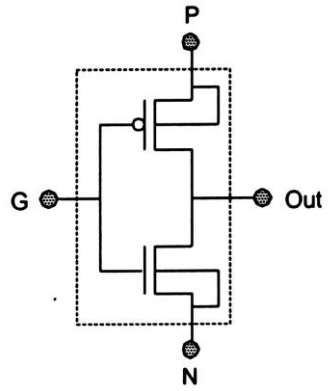

Fig .1.GDI BLOCK

It can be seen that large number of functions can be implemented using the basic GDI cell. MUX design is the most complex design that can be implemented with GDI, which requires only 2 transistors, which requires 8-12 transistors with the traditional CMOS or PTL design. Many functions can be implemented efficiently by GDI by means of transistor count.

TABLE 1
COMPARISON OF TRANSISTOR COUNT OF GDI AND STATIC CMOS [3]

Function	CMOS	GDI
Inverter	2	2
OR	6	2
AND	6	2
MUX	12	2
XOR	16	4
XNOR	16	4
NAND	4	4
NOR	4	4

Table 1 shows the comparison between GDI and the static CMOS design in terms of transistors count. It can be seen from table II that using GDI technique AND, OR, Function1, Function2, XOR, XNOR can be implemented more efficiently. However to implement NAND, NOR it requires 4 transistors as that in Static CMOS design. NAND and NOR the universal logic gates, any Boolean Function can be implemented using these gates, are most very efficient and popular with static design style[5]. Function1 and Function2 are universal set for GDI, and consists of only two transistors, compared to NAND and NOR. These functions can be used synthesize other functions more effectively than NAND and NOR gates.

B. Multi threshold CMOS(MTCMOS)

In MTCMOS, a SLEEP transistor is formed by inserting high threshold devices in series with low threshold transistors between the power supply and ground [6] as shown in fig.2. During active mode the sleep transistors are turned ON, so that the normal operation is not affected as there is a path between the supply and the ground. In standby mode the sleep transistors are turned off thereby shutting down the power supply to the circuit creating virtual supply and ground rails[7]. This technique is popularly known as SLEEP TRANSISTOR.

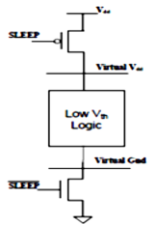

Fig .2. MTCMOS Technique

C. Low power State Retention (LPSR)Technique

The LPSR technique [8] uses a pair of NMOS and PMOS transistors above the pull up and below the pull down network of the CMOS circuit. General block diagram as well as schematics of LPSR NAND and NOR gates are as shown in fig.3. This technique has four modes of operation.

1. Active Mode: two sleep control signals namely slp = 0 and slpb = 1 are used to switch on the sleep transistors in leakage control block. Thus the virtual ground node VG is at ground potential and the virtual power node VP is at VDD[9].

2. Deep Sleep Mode: The sleep signals are held at slp = 1 and slpb = 0 states to switch off all the sleep transistors in both pull up and pull down leakage control blocks. Thus the actual power and ground path are disconnected virtually and the circuit experiences lower voltage across the nodes VP and VG.

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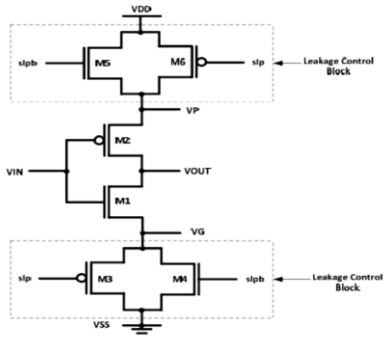

Fig.3.LPSR Technique

3. **State Retention Mode 1:** The sleep signals are given as slp = 0 and slpb = 0. The circuit sees a voltage higher than ground at the node VG and full VDD at the node VP. The state retention takes place with low leakage current with the output at good logic 1 level.

4. State Retention Mode 0: The slp = 1 and slpb=1 are given as sleep control signals. The connection to actual ground is complete, the node VP is at lower VDD. Thus the state retention takes place with low leakage current with the output at good logic 0 level.

III.IMPLEMENTATION OF DIFFERENT ADDERS USING ADVANCED POWER OPTIMIZATION TECHNIQUES

A. Half Adder

A *half adder* is a type of *adder*, an electronic circuit that performs the addition of numbers. The *half adder* is able to add two single binary digits and provide the output plus a carry value.

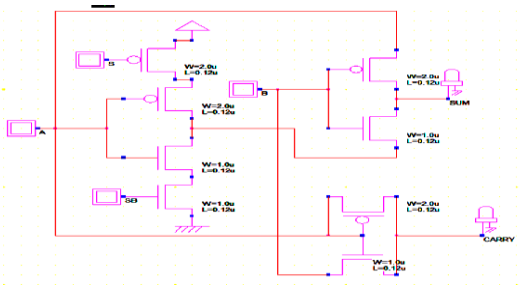

Fig.4.Half adder with MTCMOS

It has two inputs, called A and B, and two outputs S (sum) and C (carry)[3[10]]. The half adder is implemented using mux concept so that no of transistors is reduced.

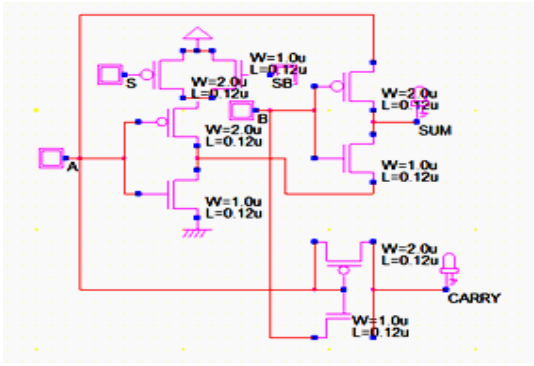

Fig .5.Half adder with LPSR technique

A.Full Adder

Full adder is a combinational circuit that performs the arithmetic sum of three bits:A,B and a carry bit C_{in}.Here full adder is implemented using the equations SUM = $\bar{C}(A \oplus B) + C(\overline{A \oplus B})$ and CARRY = $(\overline{A \oplus B})B + (A \oplus B)C$[10].The 10T full adder from the is designed with 2-input XOR, 2-input XNOR and 2-to-1 MUX, and carry is designed with 2-to-1 MUX.For the same full adder MTCMOS technique and sleep retention technique is applied and observed the power[10].

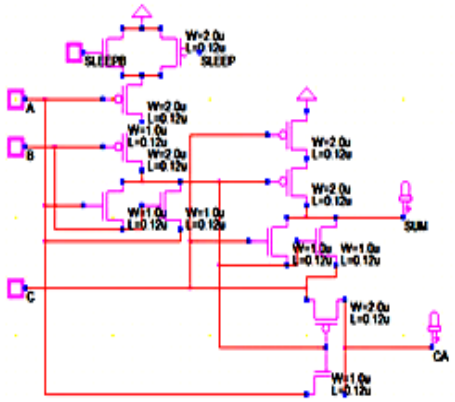

Fig.6.GDI Full adder with MTCMOS

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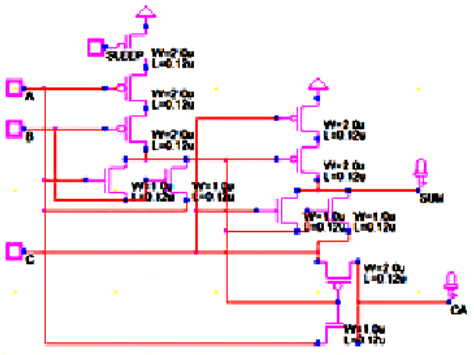

Fig.7. GDI Full Adder with LPSR technique

C.Carry Save Adder

A carry-save adder is a type of digital adder, used in computer micro architecture to compute the sum of three or more *n*-bit numbers in binary[10]. A carry save adder consists of a ladder of stand-alone full adders as shown in the fig 8. The n-bit CSA consists of n disjoint full adders (FAs) where each of which computes a single sum and carry bit based on the corresponding bits of the three input numbers. It consumes three n-bit input integers to be added and produces two outputs-bit partial sum and n-bit carry. With this adder circuit delays can be reduced. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits[11]. Carry save addition is being used in multipliers, signal processing, FFT etc

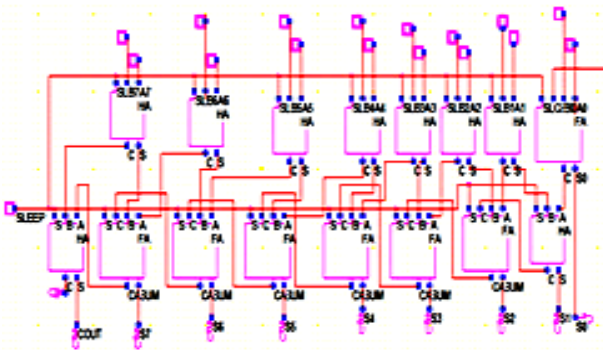

Fig.8.Carry save adder with MTCMOS

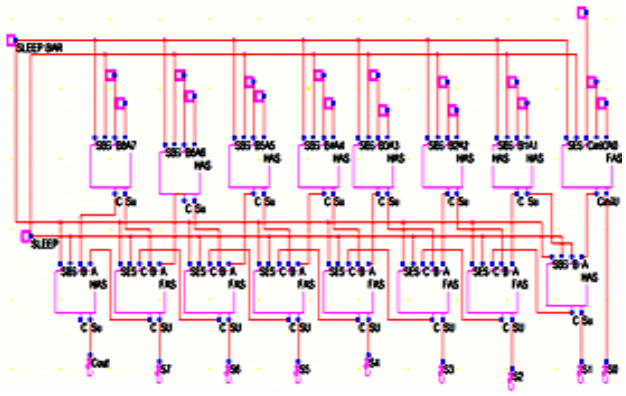

Fig.9.Carry Save Adder with LPSR technique

D.Carry Skip Adder

The Carry skip adder is a skip the logic in propagation of carry and its implementation is to speed up the additional operation and to[12] adding the propagation of carry bit around portion of entire adder. The CSKA consists of one stage containing chain of full adders (FAs) (RCA block), AND gates, OR gates.

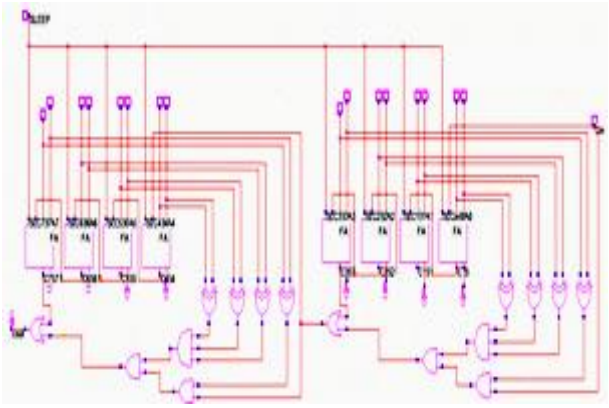

Fig.10.Carry skip adder with MTCMOS

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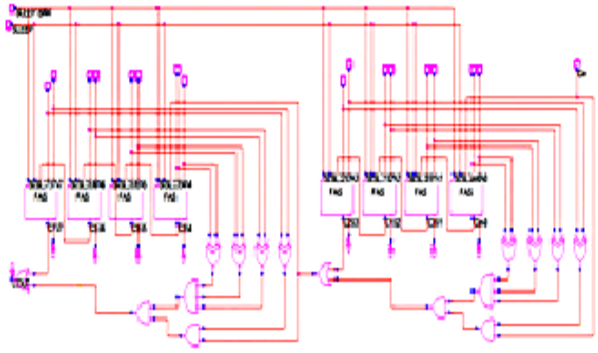

Fig.11.carry skip adder with LPSR technique

III. SIMULATION RESULTS

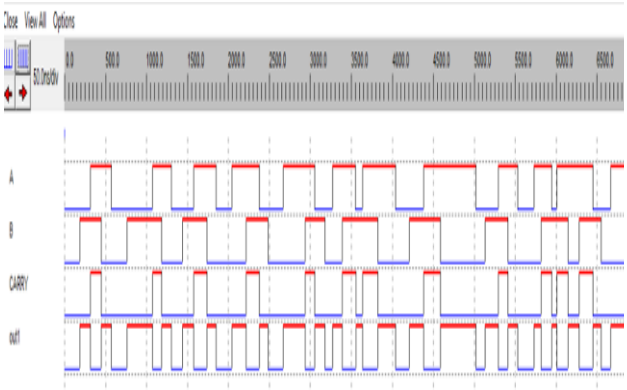

Fig.12.Half adder output

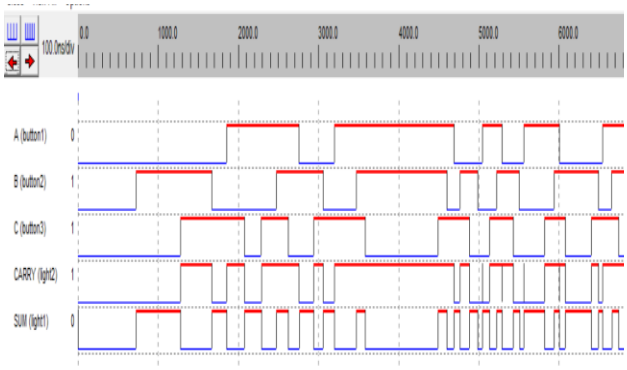

Fig.12.Full adder output

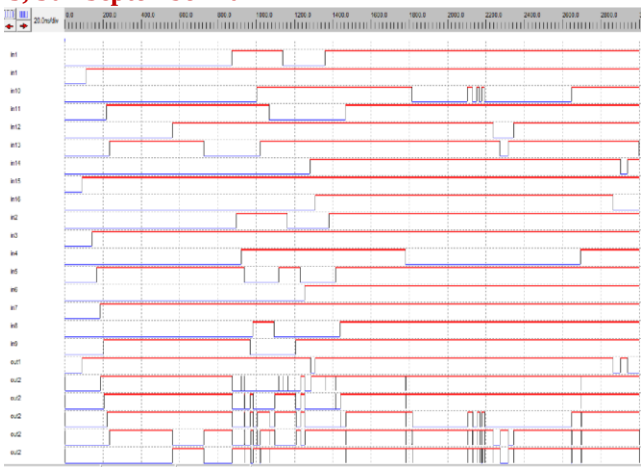

Fig.13.Carry save adder output

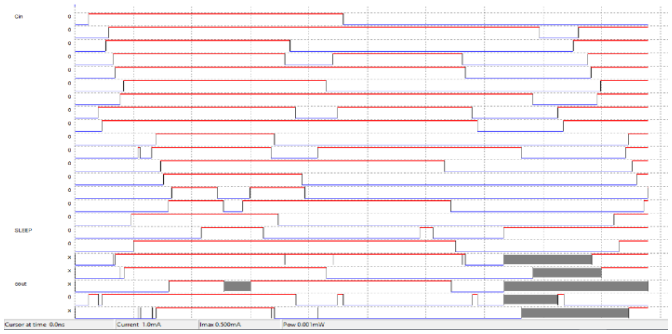

Fig.14.Carry skip adder output

V.CONCLUSION

In this paper all the adders are implemented using GDI technique and advanced power optimization techniques such as MTCMOS and STATE RETENTION are applied to the implemented adders. And also observed the power consumed at different voltages such as 3.5V,2V and 1V at 0.35 µm technology. The power at different voltages is compared with the convention CMOS logic .it is observed that power is reduced in both MTCMOS and STATE RETENTION techniques. For the observation it is concluded that ultra-low power optimization techniques are able to reduce the power than convention CMOS logic.

TABLE.3
POWER CONSUMPTION OF HALF ADDER

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HALF ADDER			
SUPPLY VOLTAGE	3.5V	2V	1V
Conventional CMOS	0.101mW	56.27µW	16.14µ
MTCMOS	27.89µW	21.63µW	13.82Mw
LPSR	36.26µW	28.85µW	20.46µW

TABLE.4
POWER CONSUMPTION OF FULL ADDERADDER

FULL ADDER			
SUPPLY VOLTAGE	3.5V	2V	1V
Conventional CMOS	0.155mw	68.24µW	18.48µW
MTCMOS	57.89µw	20.14µW	2.078µW
LPSR Technique	96.18µw	33.59µW	13.07µW

TABLE.5
POWER CONSUMPTION OF CARRY SAVEADDER

CARRY SAVE ADDER			
SUPPLY VOLTAGE	3.5V	2V	1V
Conventional CMOS	3.557mW	1.99mW	0.720mW
MTCMOS	3.057mW	0.507mW	0.148mW
LPSR Technique	3.27mW	0.67mW	0.347mW

TABLE.6
POWER CONSUMPTION OF CARRY SKIP ADDER

CARRY SKIP ADDER			
SUPPLY VOLTAGE	3.5V	2V	1V
Conventional CMOS	9.372mW	2.66mW	63.621µW
MTCMOS	4.768mW	0.790mW	30.239µW
LPSR technique	5.005mW	0.92mW	59.18µW

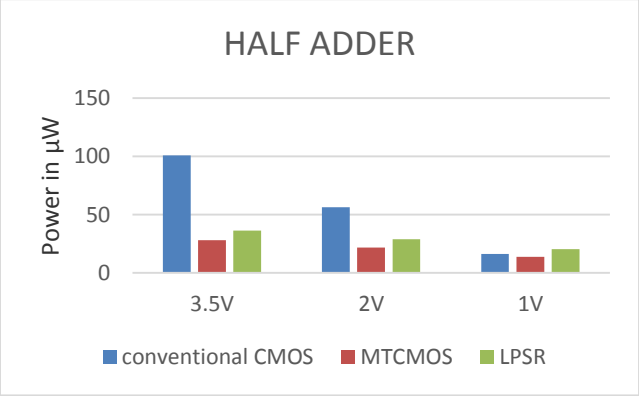

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Fig.15.Power analysis of half adder at different supply voltages

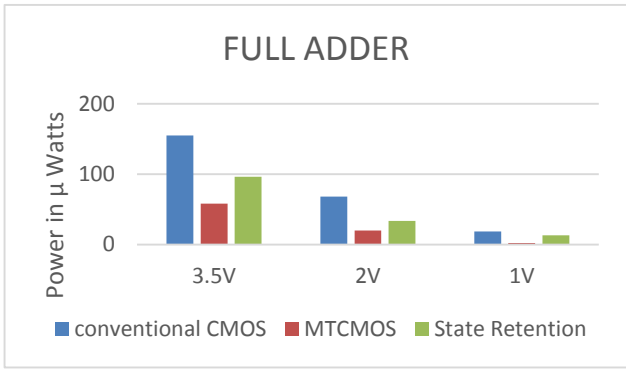

Fig.16.Power analysis of full adder at different supply voltages

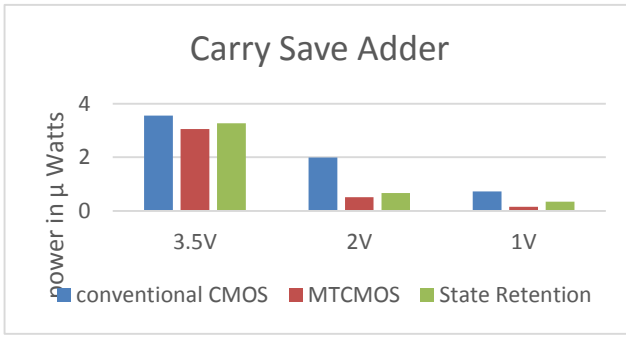

Fig.17.Power analysis of carry save adder at different supply voltages

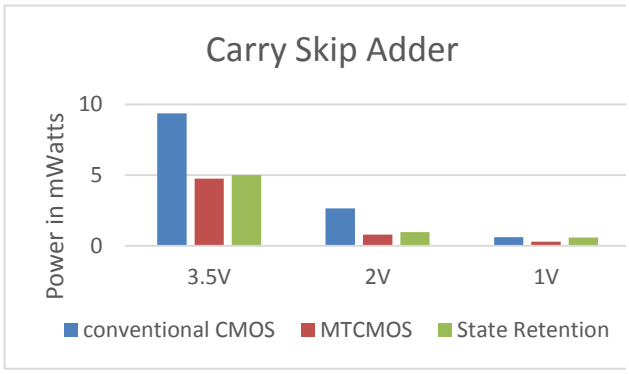

Fig.18.Power analysis of half adder at different supply voltages

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