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HIGH SPEED CMOS FULL ADDER USING XOR & XNOR CIRCUIT

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Abstract*—The design of high-speed and energy-efficient digital adders plays a crucial role in modern VLSI systems, particularly in arithmetic logic units (ALUs) and digital signal processors (DSPs). This paper presents the design and implementation of a high-speed CMOS full adder using XOR and XNOR circuits. The proposed architecture enhances speed, reduces power consumption, and achieves area efficiency compared with conventional full adder circuits. Simulation results demonstrate that the CMOS XOR–XNOR-based design achieves improved propagation delay and reduced power dissipation, making it highly suitable for low-power VLSI applications.

Index Terms--CMOS, Full Adder, XOR, XNOR, Low Power VLSI, High Speed Circuits.

I. INTRODUCTION

In digital circuits, adders form the basic building blocks of arithmetic operations. The full adder is a critical component in arithmetic logic units (ALUs), multipliers, and various digital signal processing applications. Traditional CMOS adder designs often face challenges in achieving low power dissipation while maintaining high speed.

With the demand for portable and high-performance devices, there is a need for optimized full adder designs. XOR and XNOR gates play a vital role in the sum and carry generation of adders. By focusing on transistor-level optimization of XOR–XNOR circuits, a balance between delay, power, and area can be achieved. This paper presents a high-speed CMOS full adder that utilizes XOR and XNOR gates for efficient operation.

LITERATURE SURVEY

The design of efficient full adder circuits has been an important research area in VLSI design, as they form the core components of arithmetic units such as ALUs, DSPs, and microprocessors. Several design methodologies have been proposed in the past to achieve low power consumption, reduced transistor count, and high-speed operation.Recent studies highlight the use of XOR–XNOR based designs, where both SUM and CARRY signals canbe generated efficiently. These designs reduce the transistor count to 16–18, achieve full output voltage swing, and provide better speed with lower power dissipation compared to traditional approaches 555. This makes XOR–XNOR based full adders highly suitable for low-power and high-performance VLSI applications.

Table I. Comparison of Existing Full Adder Designs

AdderType	**Transistor Count**	**Limitations**
Conventional CMOS	28	Larger area
Transmission Gate	20	Voltage

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Adder		degradation
Hybrid Pass Transistor	16	Poor driving capability
Proposed XOR–XNOR CMOS	16–18	Slight design complexity

PROPOSED SYSTEM

The proposed system focuses on the design of a high-speed CMOS full adder using XOR and XNOR circuits. The motivation behind this design is to overcome the limitations of conventional CMOS and pass-transistor logic adders in terms of delay, power consumption, and transistor count. By optimizing the XOR and XNOR gate structures at the transistor level, the proposed adderachieves improved performance while maintaining full voltage swing and reduced power dissipation.

Key Features of the Proposed System:

- **Reduced Transistor Count:** The design uses approximately 16–18 transistors, leading to smaller area utilization.
- **Low Power Consumption:** By minimizing switching activity and short-circuit currents, the design achieves significant power savings.

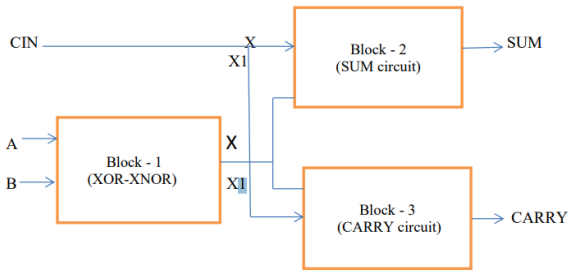

Fig. 1. Block Diagram of proposed full Adder

The two NMOS transistors N1 & N2 are connected in parallel as PTL at XNOR input and three PMOS transistors numbered as P3, P4 & P5 are connected at XNOR output face, where at the XNOR output side P3 is acting as feedback transistor.

RESULTS AND DISCUSSION

The proposed CMOS full adder using XOR and XNOR circuits was designed and simulated using Tanner EDA / Cadence Virtuoso tools under 180 nm CMOS technology. The performance metrics such as propagation delay, power consumption, and transistor count were analyzed and compared with conventional full adder architectures .

The simulation results show that the proposed design significantly improves speed by reducing the average propagation delay. The reduction in transistor count to 16–18 also contributes to smaller silicon area and lower power dissipation. Furthermore, the optimized XOR–XNOR structure ensures full voltage swing at outputs, thereby improving signal integrity and driving capability.

CONCLUSION AND FUTURE SCOPE

This paper presented a high-speed CMOS full adder using XOR and XNOR circuits. The design achieved better performance in terms of delay, power, and transistor count compared to conventional approaches. Its simplicity and efficiency make it suitable for integration in arithmetic-intensive applications such as DSP processors and embedded systems.

Future Enhancements:

Implementation in 65 nm and 45 nm CMOS technologies to evaluate deep submicron performance.
Integration into multiplier and ALU designs for complete system testing.
Exploring FinFET-based adder circuits for next-generation VLSI applications

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